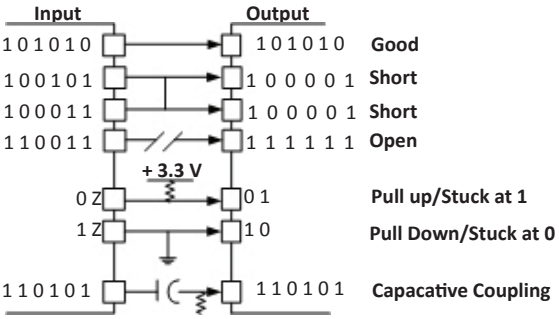
Testing for the IEEE 1149.1 JTAG / Boundary Scan Standard

onTAP ATPG - Test-to-Print

onTAP's ATPG reads CAD netlists and BSDL files to generate test programs that verify PCBs are built-to-print. Pin-level diagnostic messages pin-point faults. TAP integrity test verifies JTAG port is properly functioning.

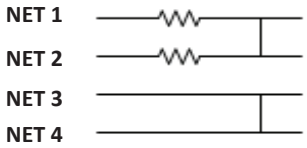
Interconnect Test

A connectivity test, or **Interconnect Test**, is the foundation of any boundary scan test solution. This test verifies that devices are properly connected to your board with no opens or shorts, especially common with BGAs. onTAP's ATPG generates test patterns to ensure that boards are free of defects including opens, stuck-ats-shorts and mid-state/resistive shorts.



Mid-state / Resistive Shorts

A major problem that often goes undetected by typical boundary scan connectivity tests is mid-state/resitive shorts. The typical connectivity tests will locate the short between nets 3 and 4, but can not locate the resistive short which exists between nets 1 and 2. This type of short is a mid-state condition, and is recognized and diagnosed by onTAP. See our application note on Interconnect testing for more information.



Bus Wire

onTAP-Specific Interconnect test manages bus wires when multiple outputs are connected to a net. onTAP verifies each pin has the chance to drive the output high and low while all inputs capture values.

Cluster Testing

onTAP uses the high-level DTS test language to develop reusable test models for testing connectivity between scan devices and non-scan devices such as DDR2, SRAM, SDRAM, and FLASH. Program FLASH memory and configure logic.