Interconnect Test

Interconnect tests are a key function of any boundary scan test program. The onTAP-Interconnect Test performs the 3 essential functions of boundary scan:

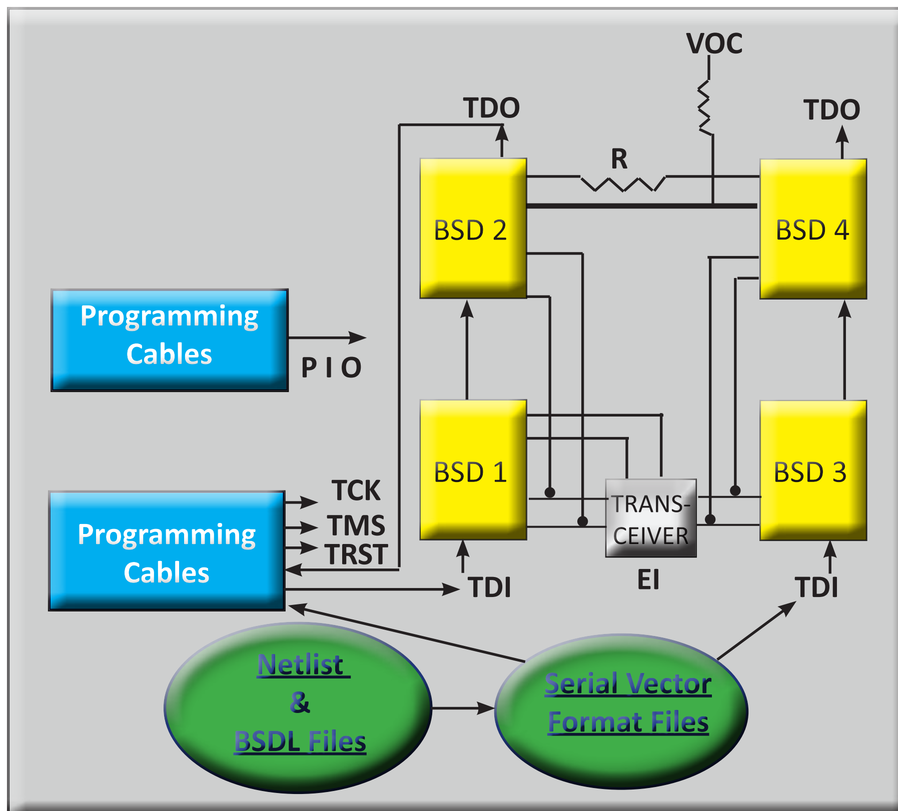
1. Confirm each component/device properly performs
2. Confirm the components/devices are properly interconnected
3. Confirm the components on the board interact correctly, and that the board performs.

(adapted from the IEEE 1149.1 spec)

The onTAP-Interconnect Test increases test fault coverage by incorporating these elements:

- ***ATPG vectors***
- ***Open circuit faults (opens) and short circuit faults (shorts)***
- ***Mid-state shorts (resistor network faults)***
- ***Pull-up/pull down resistor tests***
- ***Stuck at faults***
- ***Bus wire faults***
- ***TAP integrity***

These elements enable the development of high test fault coverage. The number and type of tests run for each element will make the fault coverage more comprehensive, creating more useful and accurate tests. The goal of any interconnect test is to test as many possible connections and interconnections, of pins and devices as possible in the process. Because board space is very limited, and usually packed with complex devices, sometimes with difficult to access pins, such as on BGAs, it is critical that boundary scan tests reach as many points as possible to return the most comprehensive, and accurate results.



Compile test from BSDL and Board netlist files for one or more JTAG chains. Tests manage devices, such as resistors and buffers that lie between Boundary Scan Pins, and Check TAPS, OPENS, SHORTS, BUS-WIRE and PULL-UP/DOWN Resistors.

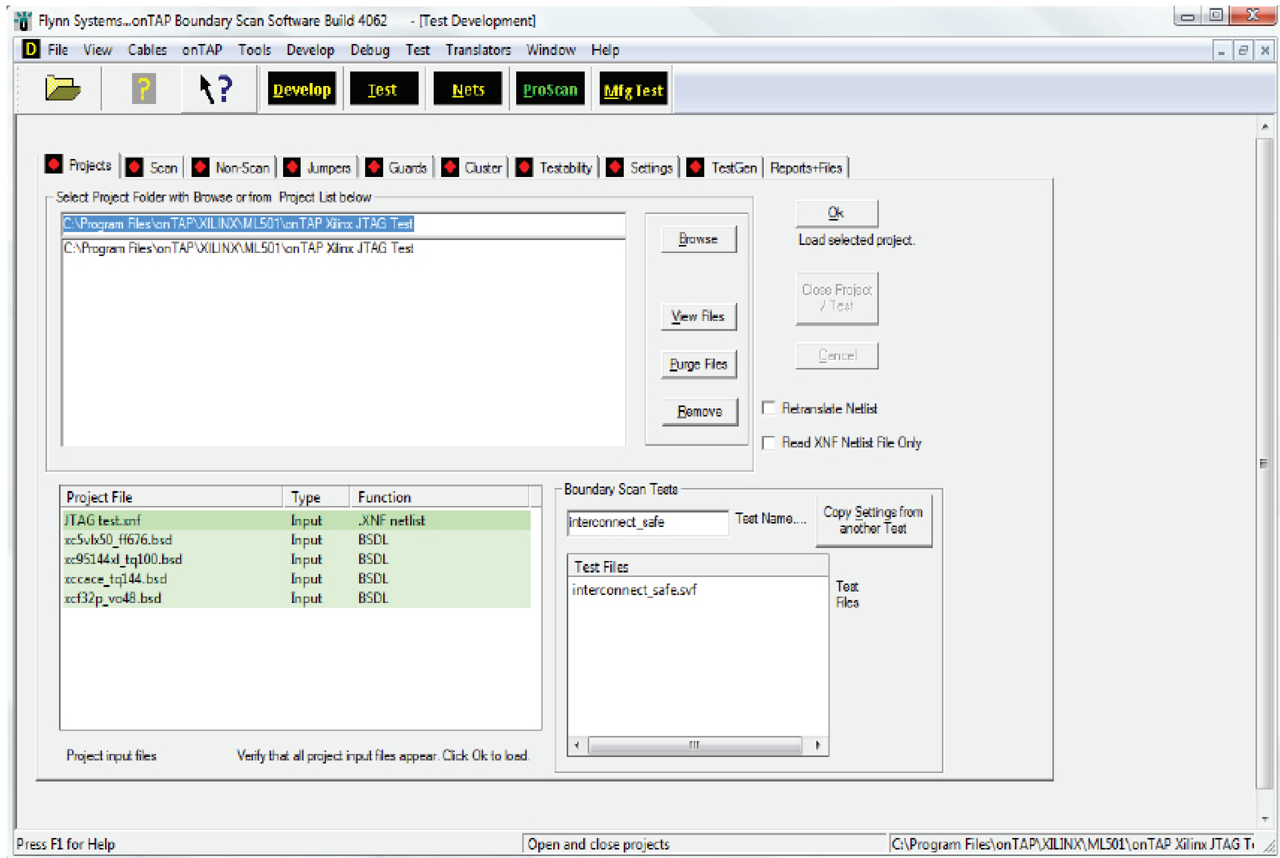
Highlights of onTAP Interconnect Tests

- Board netlist and BSDL files are comiled to creat e serial vector format files - SVF files.
- Over a dozen popular CAD readers available for netlists
- Netlist merge tool allows projects to be combined
- Checks syntax and semantics errors in BSDL
- TAP integrity tests check INSTRUCTION CAPTURE, INSTRUCTION REGISTER LENGTH, BYPASS and IDCODES.
- Connectivity between boundary scan pins on a net
- BUS-WIRE tests check stuck at drive/sense on each bus pin on a net
- PULL UP/DOWN tests for resistors
- SHORTS tests check shorts between any two or more nets with boundary scan pins or to Power and Ground.
- Run time management of buffer / transceiver enable and direction controls
- Transparency for resistor packs and two state buffers
- Static Guards control interaction and contention between non-scan logic and scannable JTAG pins
- Runs multiple interacting parallel chains simultaneously
- Scan sequencer allows one or more SVF files to be run together
- Memory and Cluster test may be run together with interconnect tests.
- Provides precise pin-level diagnostic messages for faults on boards.
- DLL available to run from third party test executives
- Run straight from ProScan control screen

All Rights Reserved

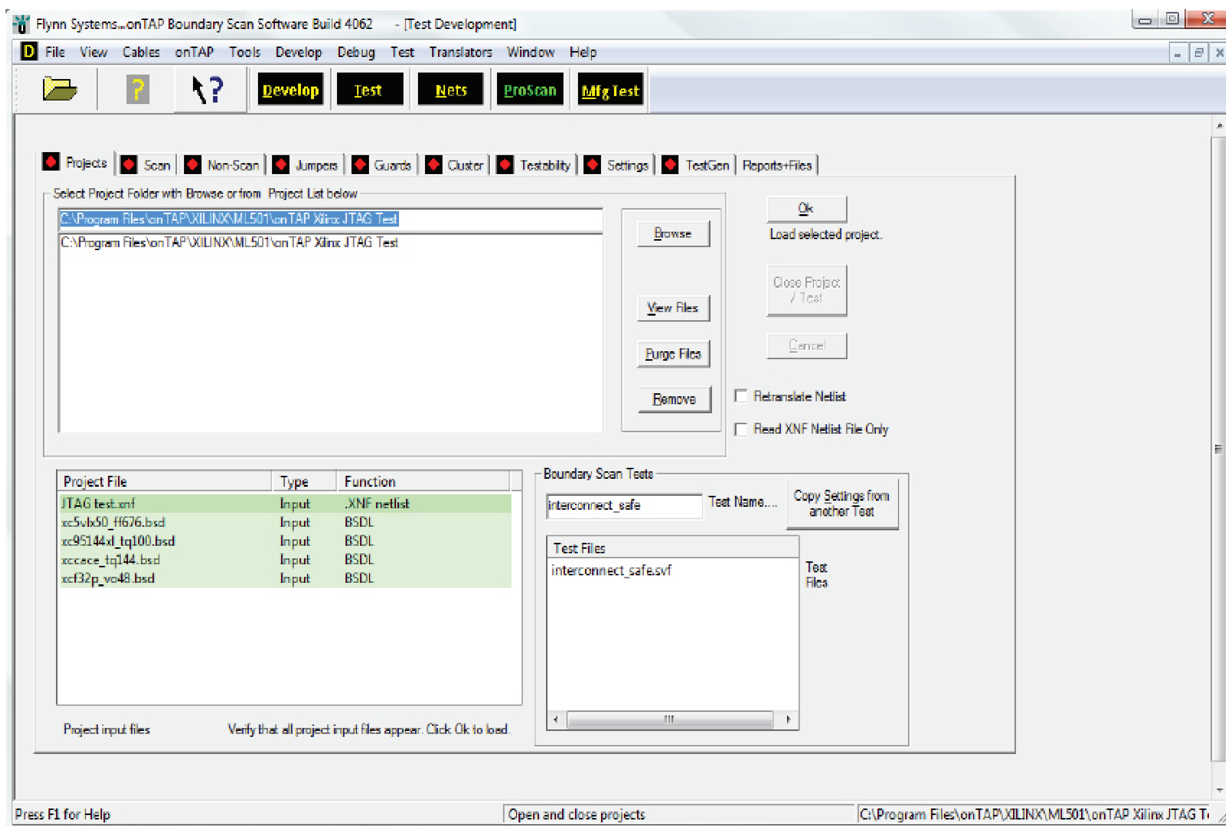
Procedure to Develop an Interconnect Test

To create a test, a netlist file and all applicable BSDL files are placed in a project folder. On the Test Development screen (yellow 'Develop' on the toolbar), a user proceeds from left to right through the tabbed pages, which help to organize and collect all of the information that onTAP requires in order to create a successful interconnect test.



onTAP Development tools compile BSDL files and board netlists into interconnect tests in the form of SVF files, which onTAP's Test executive can then apply through standard programming cables to a test board. The test development process is relatively straightforward, requiring intervention mostly to identify logic, particularly non-JTAG/non-scan devices that lie between boundary scan pins or interact with them.

All Rights Reserved



These pages and their purposes are as follows:

Projects shows input files and opens a project.

Scan facilitates matching logic locations to BSDL file names, defining JTAG chains, and performing a syntax and semantics check of each BSDL file. Errors are related to the controlling IEEE 1149.1 paragraph.

Non-scan identifies power and ground nets as well as non-boundary scan logic that may be selected to create memory/flash/cluster test models.

Jumpers connects up JTAG chains as required and makes devices between boundary scan pins transparent.

Guards helps set static values that protect boundary scan pins from contention with non-boundary scan pins, e.g., an SRAM connected
to an FPGA.

Cluster facilitates simple identification of Cluster Test Model, pin assignment of non-scan devices, and correlating scan pins.

Testability warns of testability conditions that could prevent successful development, e.g., JTAG COMPLIANCE pins that are not held at the correct values.

Settings allows selection from many options such as ground-debounce.

TestGen allows selection of test procedures, e.g., INTERCONNECT or BYPASS for selected devices, and initiates the automatic test generation process.

All Rights Reserved

Procedure to Run an Interconnect Test

Once a test has been developed, its SVF file may be run simply by proceeding directly to the Test screen (yellow ‘Test’ on the toolbar), browsing to it, and clicking the Go button.

Test Files

When a test is developed several critical files are created, including a Serial Vector Format (.SVF) file that contains the test, an .SVX file that contains diagnostic information, and a report file called TestabilitySurvey_testfile.txt. The TestabilitySurvey file shows opens/shorts fault coverage for all pins on a board and also provides a summary score.

Debug Tools

Debug tools may generally be accessed from the Debug menu list, the Test screen, or the ProScan menu. Some of the debug tools are:

- **Examine SVF** parses SVF files and shows drive/sense values for all pins at each SVF scan vector. Test failures are overlayed to help show test activity in the context of boundary scan pin activity.
- **LOG HEX DATA** “dumps” all measured TDI , TDO, and MASK activity to a file.
- **LOOP** repeats tests so that repeating test activity may be observed.
- **Breakpoints and Single Step** allow tests to be stopped at specific scan vectors so that measurement can be made.
- **Trace** allows selected scans, particularly for memory/cluster tests, to be written, along with all variable values to a specified file for analysis.
- **Scan Disables** turns off test for selected scans, to facilitate debug of others.

All Rights Reserved