Interconnect Test

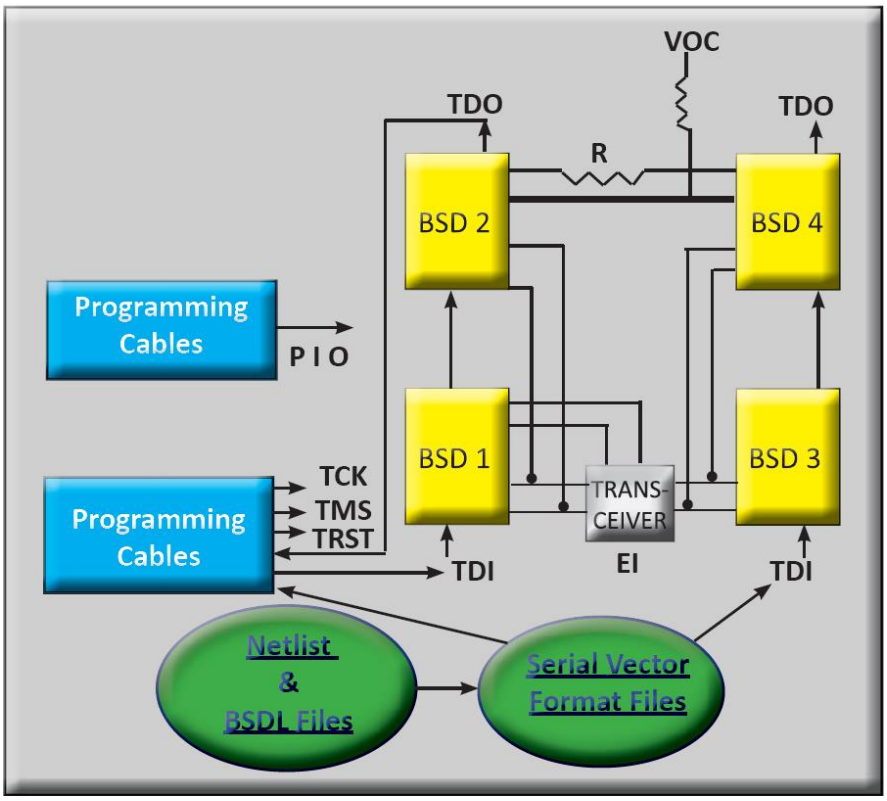
Interconnect tests are a key function of any boundary scan test program. The onTAP-Interconnect Test performs the 3 essential functions of boundary scan:

1. Confirm each component/device properly performs
2. Confirm the components/devices are properly interconnected
3. Confirm the components on the board interact correctly, and that the board performs. (adapted from the IEEE 1149.1 spec)

The onTAP-Interconnect Test increases test fault coverage by incorporating these elements:

- ***ATPG vectors***
- ***Open circuit faults (opens) and short circuit faults (shorts)***
- ***Mid-state shorts (resistor network faults)***
- ***Pull-up/pull down resistor tests***
- ***Stuck at faults***
- ***Bus wire faults***
- ***TAP integrity***

These elements enable the development of high test fault coverage. The number and type of tests run for each element will make the fault coverage more comprehensive, creating more useful and accurate tests. The goal of any interconnect test is to test as many possible connections and interconnections, of pins and devices as possible in the process. Because board space is very limited, and usually packed with complex devices, sometimes with difficult to access pins, such as on BGAs, it is critical that boundary scan tests reach as many points as possible to return the most comprehensive, and accurate results.



Compile test from BSDL and Board netlist files for one or more JTAG chains. Tests manage devices, such as resistors and buffers that lie between Boundary Scan Pins, and Check TAPS, OPENS, SHORTS, BUS-WIRE and PULL-UP/DOWN Resistors

Highlights of onTAP Interconnect Tests

- Board netlist and BSDL files are compiled to create serial vector format files - SVF files.
- Over a dozen popular CAD readers available for netlists
- Netlist merge tool allows projects to be combined
- Checks syntax and semantics errors in BSDL
- TAP integrity tests check INSTRUCTION CAPTURE, INSTRUCTION REGISTER LENGTH, BYPASS and IDCODES.
- Connectivity between boundary scan pins on a net
- BUS-WIRE tests check stuck at drive/sense on each bus pin on a net
- PULL UP/DOWN tests for resistors
- SHORTS tests check shorts between any two or more nets with boundary scan pins or to Power and Ground.
- Run time management of buffer / transceiver enable and direction controls
- Transparency for resistor packs and two state buffers
- Static Guards control interaction and contention between non-scan logic and scannable JTAG pins
- Runs multiple interacting parallel chains simultaneously
- Scan sequencer allows one or more SVF files to be run together
- Memory and Cluster test may be run together with interconnect tests.
- Provides precise pin-level diagnostic messages for faults on boards.
- DLL available to run from third party test executives
- Run straight from ProScan control screen