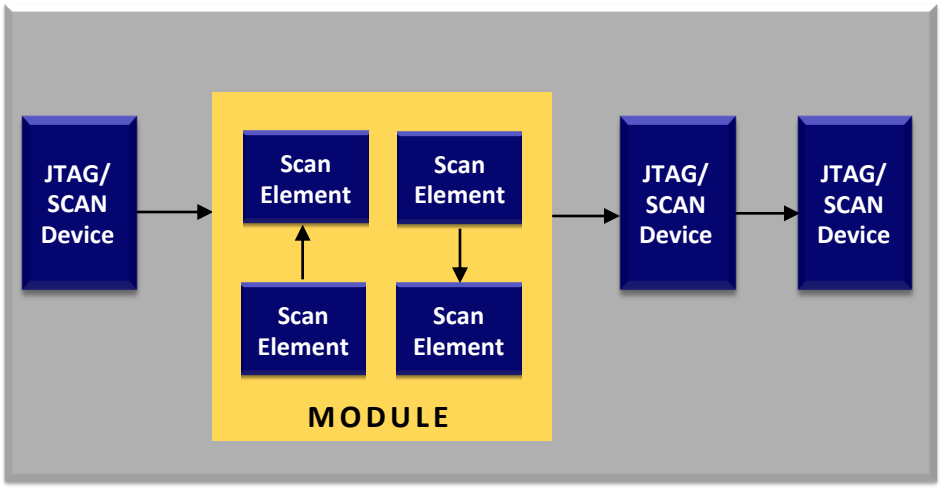
Managing Multi-Chip Modules

Decreasing real estate on boards has increased the popularity of modules (devices containing multiple boundary scan elements inside one package) in boundary scan applications. These devices can pose problems when designing and testing because all scan elements on the module must be tested. onTAP provides an easy solution for incorporating modules in tests. With onTAP's "auto chain detection" and netlist merge tools, onTAP quickly and easily detects the module, interrogates its netlist, and enables you to incorporate modules in tests, which in turn, expands and increases test fault coverage.

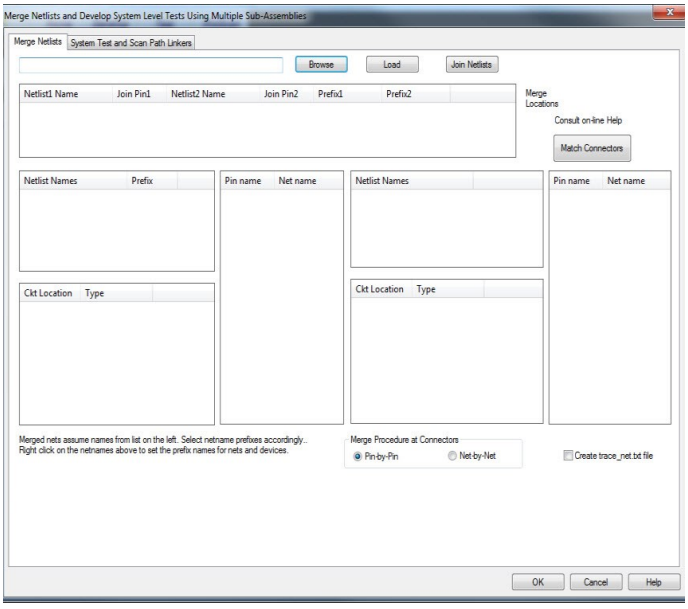
Highlights: Managing Modules

- Utilize built-in test development functions to include modules in test development
- Boost fault coverage
- Expand test capability



Detecting & Testing the Module

Achieving the most comprehensive fault coverage when modules appear in JTAG scan chains is imperative to achieving good JTAG tests. Modules appear as a hole in the scan chain, making testing more difficult. onTAP can recognize these holes as modules and incorporate them into the test with some simple procedures. This can all be accomplished during test development using onTAP's built-in tools.



Managing Modules - Application

Using the PLX Technology PEX 8311 PCI Bridge as an example, solutions involving multi-chip modules (MCM) may be created as shown in the following procedure. In the example, a netlist in Allegro format (.DAT file) and BSDL files for each module serve as input files for the MCM.

onTAP creates an initial solution for just the MCM and creates a .XNF netlist. This XNF netlist is then merged with an XNF netlist for the target board, created when onTAP opens the board-level project. The two XNF netlists, target board and MCM, are merged using the onTAP Merge Netlists tool, and then the merged netlist and all BSDL files are placed in a new folder and are ready for test development.

The steps to merge PEX modules to a board are as follows:

- Place the PEX 8311 .DAT netlist and the board netlist in a folder.
- Change the .DAT extension to .NET so onTAP can read the Allegro format.
- If more than one PEX circuit location exists on the board, then a separate PEX netlist must be established for each circuit location. This can be done by simply saving the PEX netlist with a unique filename for each location.
- Open the onTAP Tools/Merge Netlists tool and proceed as follows:
  1. Browse to the merge folder and Load the netlists.
  2. In the Netlist Names list on the left, right click on each netlist and assign a unique prefix for each netlist, e.g., pex_u1_. The board netlist can be assigned a null prefix.
  3. Select the board netlist on the left list of Netlist Names, and select a PEX circuit location.
  4. Select the corresponding PEX netlist from the Netlist Names list on the right, and select the BALL Circuit Location.
  5. Select “Match Connectors”.
  6. Repeat steps 3-5 for each PEX device.
- Select Join Netlists
- Move the merged_netlist.xnf to a new folder along with all of the BSDL files and run the project. On the Scan page, the two PEX BSDL files can be matched to the corresponding PEX and PCI locations for each PEX module.

If a netlist is not available for the MCM, the following procedure can be used.

MultiChipModule.txt

This file must be created by the user prior to opening a project. MCMs may be used to handle devices with multiple JTAG sections such as TI’s TMS320VC5441. The format entries map a device’s circuit location to multiple new sub locations and bsdl file names. A .XNF netlist is created that shows the sub locations with JTAG pins apportioned according to the bsdl file assignments.

Sample file entries, assuming that board location U1 is a TMS320VC5441, follows;

U1:U1A:5441_GGU_A.BSM // U1 becomes U1A,first sub- device
U1:U1B:5441_GGU_B.BSM // second sub-device
U1:U1C:5441_GGU_C.BSM // third sub-device
U1:U1D:5441_GGU_D.BSM // fourth sub-device

Additional entries can be made for more MCMs.