



Prices and Ordering Information

Flynn Systems offers the FS-ATG Test Vector Generation Service as an economical way to get test vectors for your immediate PLD and FPGA testing needs. This document contains the following information:

1. Test Vector Generation Service Pricing.
2. Listing of devices supported in FS-PLD Libraries.

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(1) Test Vector Generation Service Pricing

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Service Runs are charged individually by device as follows:

Library	Source Files Required	Price
PLD Library 1	(.JED)	\$125
PLD Library 2	(.JED)	\$125
PLD Library 3	(.JED)	\$125
PLD Library 4	(.JED)	\$125
Actel ACT1	(.EDN & .PIN)	\$350
Actel ACT2	(.EDN & .PIN)	\$350
Actel ACT3	(.EDN & .PIN)	\$350
Actel 1200XL	(.EDN & .PIN)	\$350
Actel 3200DX	(.EDN & .PIN)	\$350
Actel MX	(.EDN & .PIN)	\$350
Actel SX	(.EDN & .PIN)	\$350
Altera MAX 5000	(.EDO)	\$350
Altera MAX 7000	(.EDO)	\$350
Altera MAX 9000	(.EDO)	\$350
Altera FLEX 6000	(.EDO)	\$350
Altera FLEX 8000	(.EDO)	\$350
Altera FLEX 10K	(.EDO)	\$350
Cypress Flash370	(.RPT)	\$350
Lattice isp/Lsi 1000	(.SIM)	\$350
Lattice isp/Lsi 2000	(.SIM)	\$350
Lattice isp/Lsi 3000	(.SIM)	\$350
Lattice isp/Lsi 6000	(.SIM)	\$350
Lucent ORCA	Call for latest info	
QuickLogic pASIC1	(.EDO)	\$350
QuickLogic pASIC2	(.EDO)	\$350
QuickLogic pASIC3	(.EDO)	\$350

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Xilinx XC2000	(.XNF)	\$350
Xilinx XC3000	(.XNF)	\$350
Xilinx XC4000	(.EDN or .XNF)	\$350
Xilinx XC5200	(.XNF)	\$350
Xilinx XC7000	(.EDN or .XNF)	\$350
Xilinx XC9500	(.EDN or .XNF)	\$350
Xilinx CoolRunner	(.ANN/FIT)	\$350
Xilinx Spartan	(EDN)	\$350
Vantis MACH 1	(.VHD & .XRF) (or .JED)	\$350
Vantis MACH 2	(.VHD & .XRF) (or .JED)	\$350
Vantis MACH 3	(.VHD & .XRF)	\$350
Vantis MACH 4	(.EDN or .VHD & .XRF)	\$350
Vantis MACH 5	(.EDN or .VHD & .XRF)	\$350

The FS-ATG Test Vector Generation Service includes:

Fault Coverage:

Generation of package pin and/or internal node Stuck-At faults.

Testability Reports:

Detailed reports of the device performance, fault-scoring summaries, DFT information, state-transition information, logic analysis, and edge-pin summary.

Test Vectors in your ATE Format:

Output Formats include GenRad, HP, Teradyne, and other ATE formats.



How to get started

 To get started, please send us your device source files (see list of source files) and either tell us how the devices are constrained (pins connected/ignored), and tied to VCC/GND or send us the board netlist file (GenRad .CKT, HP board, or Teradyne IPL.DAT). FS-ATG software extracts that information automatically for each device on your board.

Send files via email to support@flynn.com

We'll set them up on the first available PC in our lab.
 In most cases, you can expect results within 24 hours.

 (2) Listing of FS-ATG supported PLD Devices

 This is a listing of the devices in each FS-ATG PLD Library.

PLD Library 1

8L14A	10L8	16C1	16R4	18P8	PLS103
10E301	12H6	16H2	16R4Z	19L8	PLS153
10E302	12L6	6L2	16R6	20L2	PLS173
10H8	12L10	16L6	16R8	20L8	100E301
10H16P8	14H4	16L8	16RD8	20L10	100E302
10H20EG8	14L4	16P4	16RP8	22P10	10016RD8
10H20EV8	14L8	16P8	18L4	PLS100	

PLD Library 2

16RA8	20G10	20RS10	20X8	5C032	PLS155
16V8	20R4	20S10	20X10	85C220	PLS159
16V8A	20R6	20V8	20XV10	85C224	PLS167
18CV8	20R8	20V8A	22V10	EP310	PLS168
18G8	20RA10	20VP8	22VP10	EP320	PLS179
18V8	20RS4	20V10	24V10	F839	PLX448
18V10	20RS8	20X4	5C031	PLS105	

PLD Library 3

5AC312	26V12	5C090	CYP330	EP600	PLHS501
5AC324	29M16	5C180	CYP331	EP910	PLUS405
23S8	29MA16H	ATV750	CYP332	EP900	TIPLS506
26CV12	5C060	CE610	CYP335	EP1800	

PLD Library 4

ATV2500	32VX10	PA7024(Peel)	GAL6001	GAL6002B
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